Amendments to the Specification:

Please replace paragraph beginning on page 11, line 16 with the following amended paragraph:

As to operation, in one embodiment of the invention, address overload mechanism 20 generates a pair of distinct addresses from the address that is provided on address bus 203. In one embodiment of the invention, the address data on address bus 203 may be coupled from an address comparator (not shown) that is included in, or operates in conjunction with, memory controller 104. One of the addresses at the output of address multiplexer [[20]] 201 is mapped to unprotected memory ~~207~~ 108, and is coupled to unprotected memory 108 via address path 205. By virtue of the operation of address translator 211, a second address is mapped to protected memory ~~206~~ 107, and is coupled to memory 107 via address path 204. The respective outputs of memory 107 and memory 108 are coupled to data multiplexer 202 at inputs 202a and 202b, respectively. In this manner, signal 210, provided by trust co-processor 110, may be used to selectively determine which address space, 108 or 107, is accessed. That is, if signal 210 = T, then protected memory 107 is accessed; if signal 210 = $\overline{T}$, then unprotected memory 108 is accessed.

Please replace paragraph beginning on page 13, line 3 with the following amended paragraph:

FIG. 3 is a flow chart that depicts the manner in which multiple-mapped memory may be controlled and managed in accordance with an embodiment of the present invention. It must be understood here that the method flow and sequence illustrated graphically in FIG. 3 is intended to be ~~emplemplarly~~ exemplary, rather than definitive, with respect to the invention. For example, methods that exclude, or include certain additional, steps may nonetheless be captured by the scope of the subject invention. In addition, the sequence of steps may depart from that which is illustrated in FIG. 3.